REMARKS

Claims 1, 3, 4, 6, 7, 9, 10 and 12-14 are pending in the application and stand rejected. In light of the following remarks, applicant earnestly solicits favorable consideration.

Incorporation by Reference

The examiner states that as applicants have not responded to the "incorporation by reference issue," the objection is maintained. However, in the office action dated September 2, 2008, the examiner never officially issued an objection for the above stated reason.

Further, applicant is not relying on the foreign application to overcome any rejection or objection at this point.

On the Merits

Claim Rejections - 35 U.S.C. § 102(e)

Claims 1, 3, 4, 6, 7, 9, 10 and 12-14 stand rejected under 35 U.S.C. § 102(e) as being anticipated by *Vigoda et al.* (US 7,209,867), hereinafter referred to as *Vigoda.*

Independent Claim 1:

Independent claim 1 recites:

> A nonlinear controller comprising: a first module composed of a nonlinear system for creating a synchronous state with a controlled object through a nonlinear interaction with the controlled object; and
>
> a second module composed of a feedback system for adjusting a parameter to vary a relation value of the first module relating to the synchronization with the controlled object based on a difference between the relation value and a target relation value, wherein the controlled object is controlled by convergence of the relation value relating to the synchronization of the first module to the target relation value, and
>
> the first module vibrates at different natural frequencies from the controlled object, and the nonlinear interaction has an entrainment effect.

The examiner contends that the features recited above are disclosed by *Vigoda*, which is directed to "Analog Continuous Time Statistical Processing." (Title.) Applicant respectfully traverses this rejection and submits that *Vigoda* is not analogous art with respect to the claimed invention.

Addressing the specifics of claim 1, the examiner contends that a nonlinear controller is disclosed by a phase lock loop, as recited in column 2, line 9. The examiner contends that a first module composed of a nonlinear system is disclosed by a comparator, within the phase lock loop. That is, the examiner contends that a comparator is a nonlinear system.

It is unclear how the examiner considers a comparator to be a nonlinear system. That is, a comparator typically has two inputs and one output. The output is either high or low depending on the input signals. As such, a comparator could not be considered a nonlinear system, as suggested by the examiner.

Regarding the next feature of claim 1, a nonlinear system for creating a synchronous state with a controlled object through a nonlinear interaction with the controlled object, the office action appears to be silent with respect to this feature. Further, there is not any controlled object disclosed or discussed in *Vigoda*.

The examiner may contend that the voltage controlled oscillator (VCO) is the controlled object, however, applicant simply cannot discern how the examiner is interpreting the reference. Applicant asks the examiner to further clarify this position in any future correspondence.

Additionally, *Vigoda* does not disclose any "synchronous state" with a controlled object. If the examiner does consider the VCO to be the controlled object, the interaction between the VCO and the comparator would not constitute a synchronous state, as recited by claim 1.

The examiner contends that the second module is disclosed by a low pass filter. I.e., see the reference the examiner provides entitled: "Modern Electronic Communication," specifically

on page 209 which shows a diagram of a phase lock loop. Please note that the low pass filter is connected to the phase comparator in FIGURE 6-12.

Applicant notes that the purported second module (i.e. low pass filter) is part of a feedback system, in conjunction with a voltage controlled oscillator (VCO). However, the low pass filter is not itself composed of a feedback system, as recited by claim 1.

Finally, regarding the last feature of claim 1, formerly claim 2, claim 1 recites that the first module "vibrates" at different natural frequencies than the controlled object. Thus, the first module and the controlled object vibrate. As *Vigoda* is simply an electronic circuit, it does not disclose any vibration occurring at either the alleged first module (i.e. comparator,) or any alleged controlled object.

That is, electronic components in a circuit can perhaps be said to manipulate an *oscillating* signal, but the components themselves should not be said to vibrate. This would be an unreasonable characterization of the reference.

Even more so, *Vigoda* does not disclose that the alleged vibrations between the two components create an entrainment effect. An entrainment effect is described on page 5, paragraph [0014]:

> Here, an entrainment effect is a process of mutual adaptation of dynamics between different nonlinear vibrations and a phenomenon in which nonlinear vibrations with different frequencies spontaneously reach a synchronous state through an interaction.

As is apparent from the above recited passage, an entrainment effect is not disclosed by a phase lock loop.

As such, applicant respectfully requests the examiner to withdraw the rejection and allow the application.

Independent Claim 13:

As indicated above with respect to independent claim 1, applicant respectfully submits that the examiner's rejections are not appropriate.

Specifically, *Vigoda* does not disclose an object that is being controlled, as discussed above regarding claim 1. The office action appears to be silent with respect to this feature.

Furthermore, *Vigoda* does not disclose any "synchronous state" with a controlled object.

Claim 13 also recites acquiring a state variable relating to a dynamic behavior of the controlled object. No such variable is disclosed in *Vigoda*.

In short, a phase lock loop is not capable of disclosing the features recited in claim 1 or claim 13.

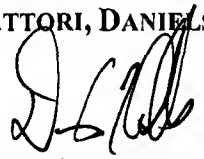
In view of the above, Applicants respectfully submit that their claimed invention is allowable and ask that the rejection under 35 U.S.C. §102 be reconsidered and withdrawn. Applicants respectfully submit that this case is in condition for allowance and allowance is respectfully solicited.

If any points remain at issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the local exchange number listed below.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP



Dennis M. Hubbs
Attorney for Applicants
Registration No. 59,145
Telephone: (202) 822-1100
Facsimile: (202) 822-1111

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